

FIG. 1A
(PRIOR ART)

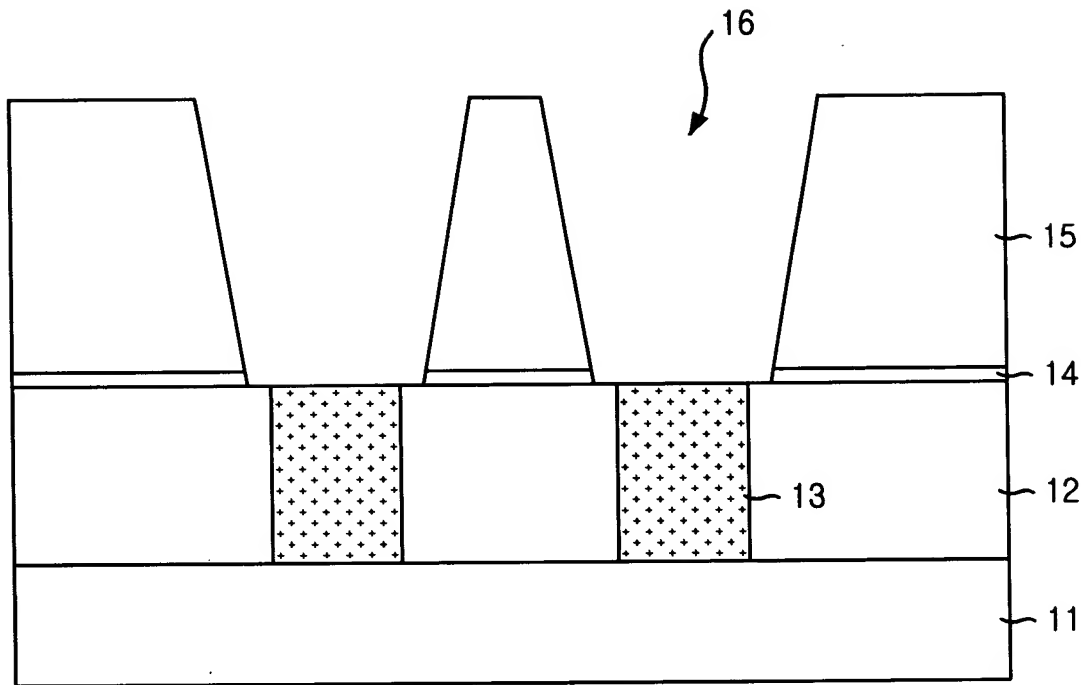


FIG. 1B
(PRIOR ART)

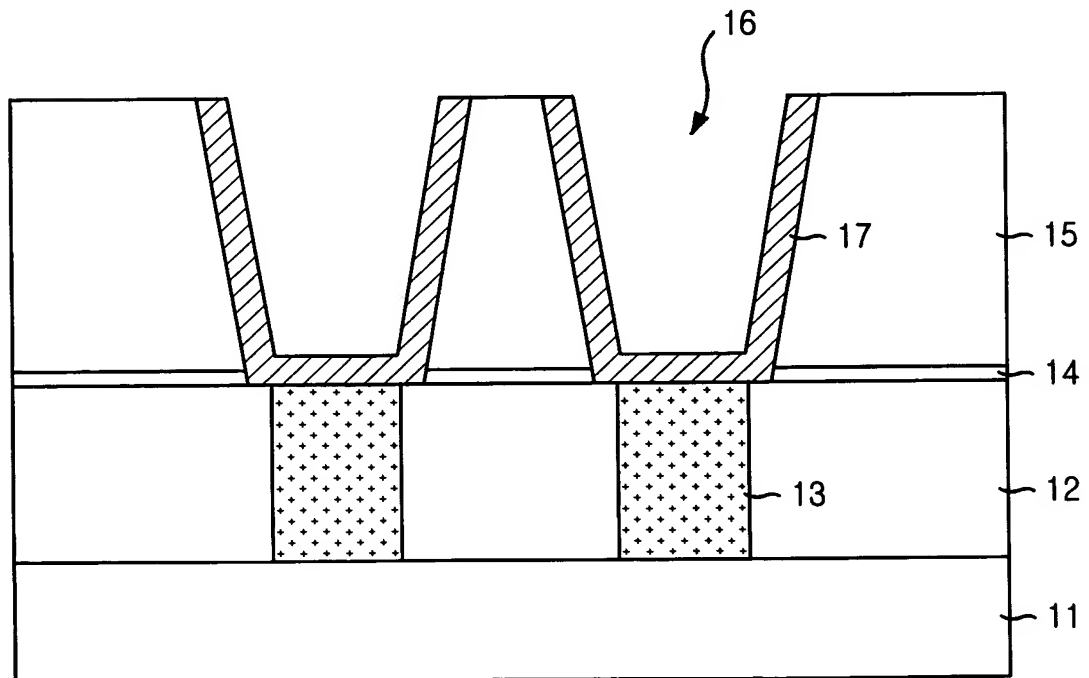


FIG. 1C
(PRIOR ART)

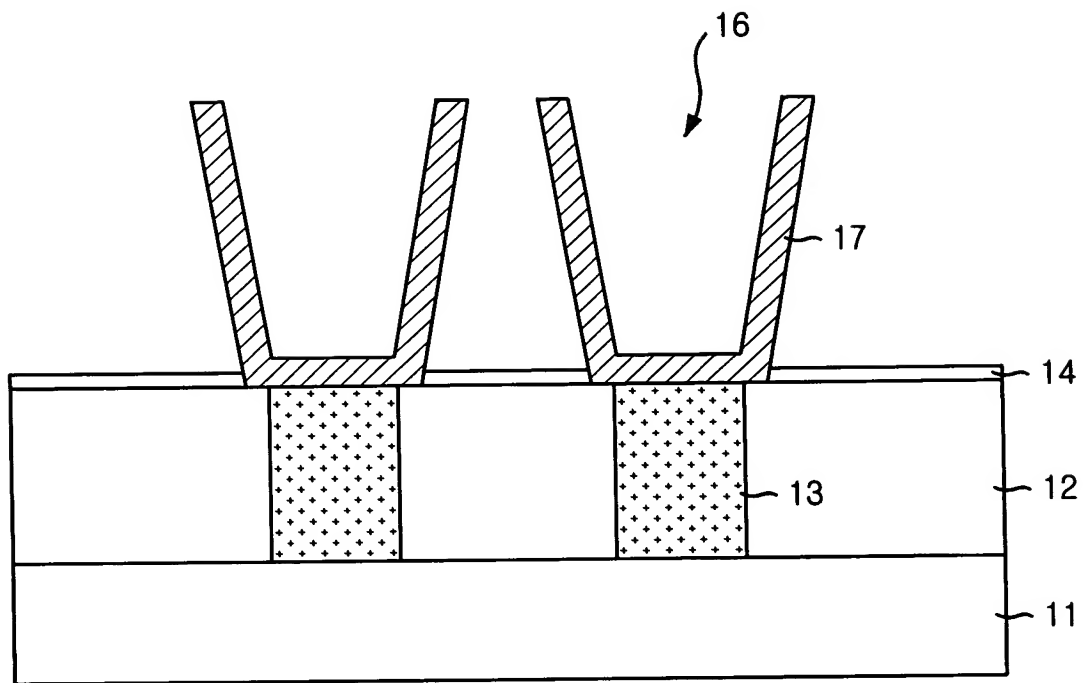


FIG. 2A
(PRIOR ART)

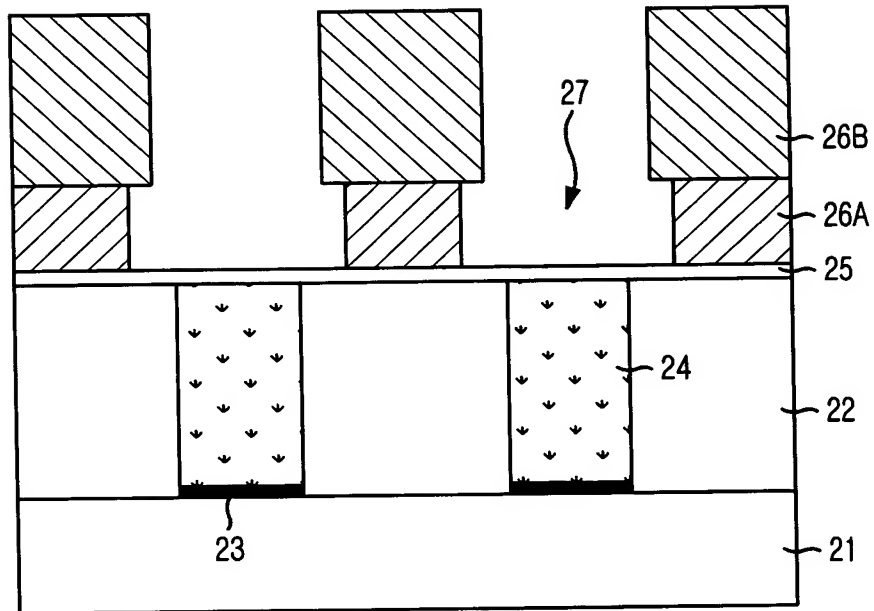


FIG. 2B
(PRIOR ART)

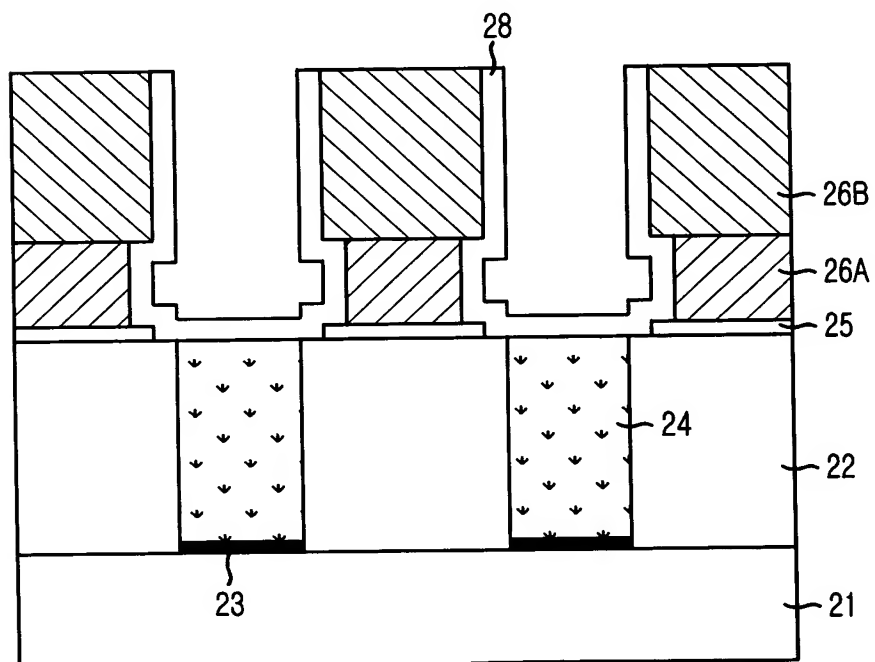


FIG. 2C
(PRIOR ART)

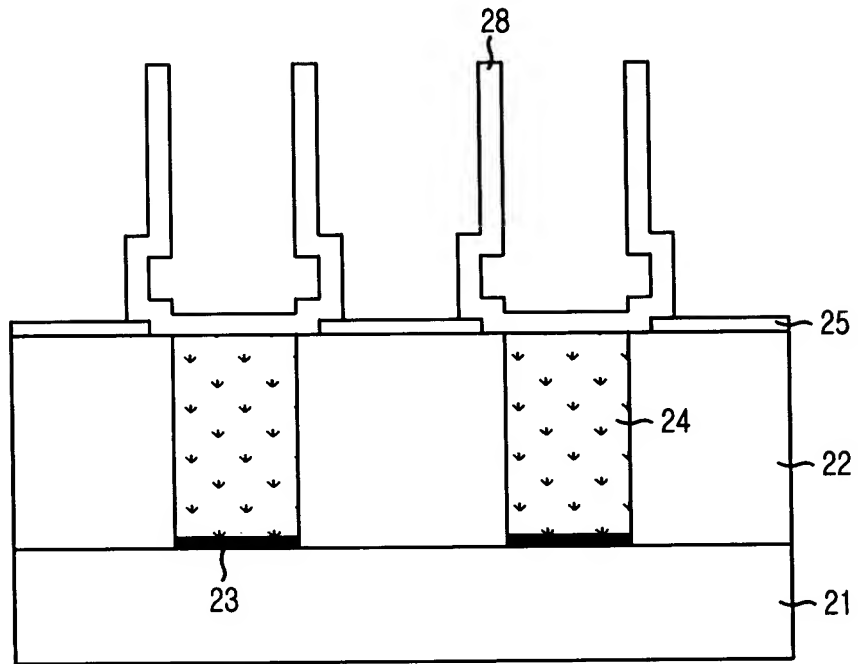


FIG. 3

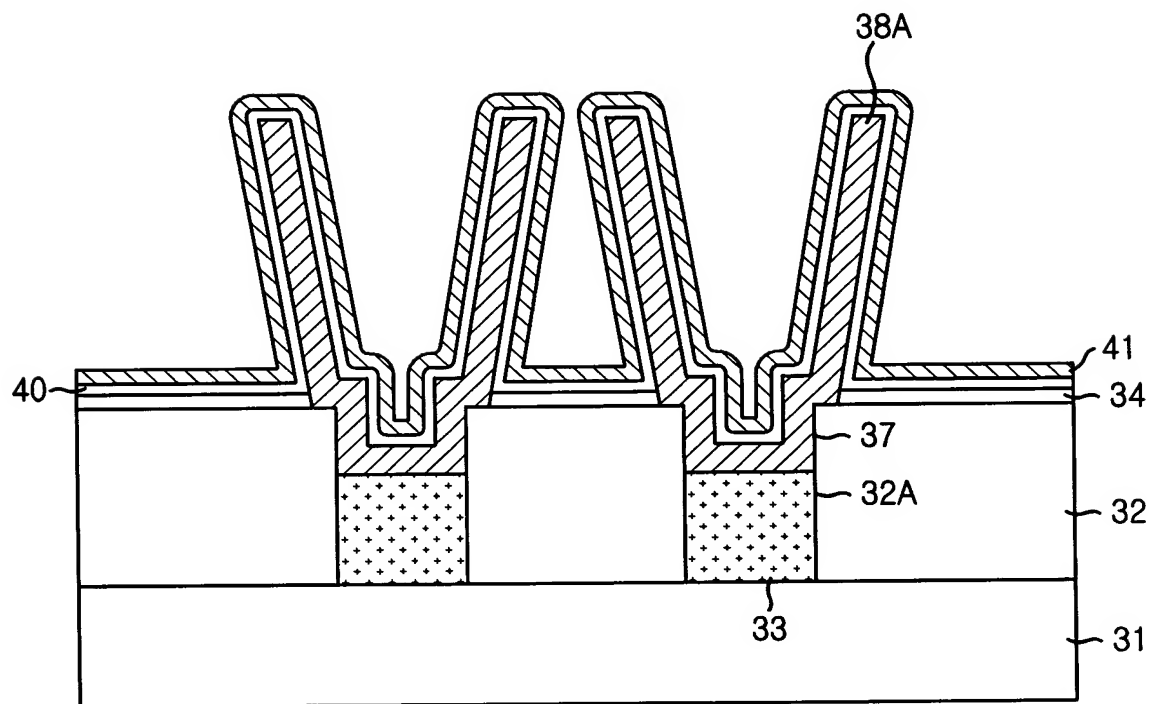


FIG. 4A

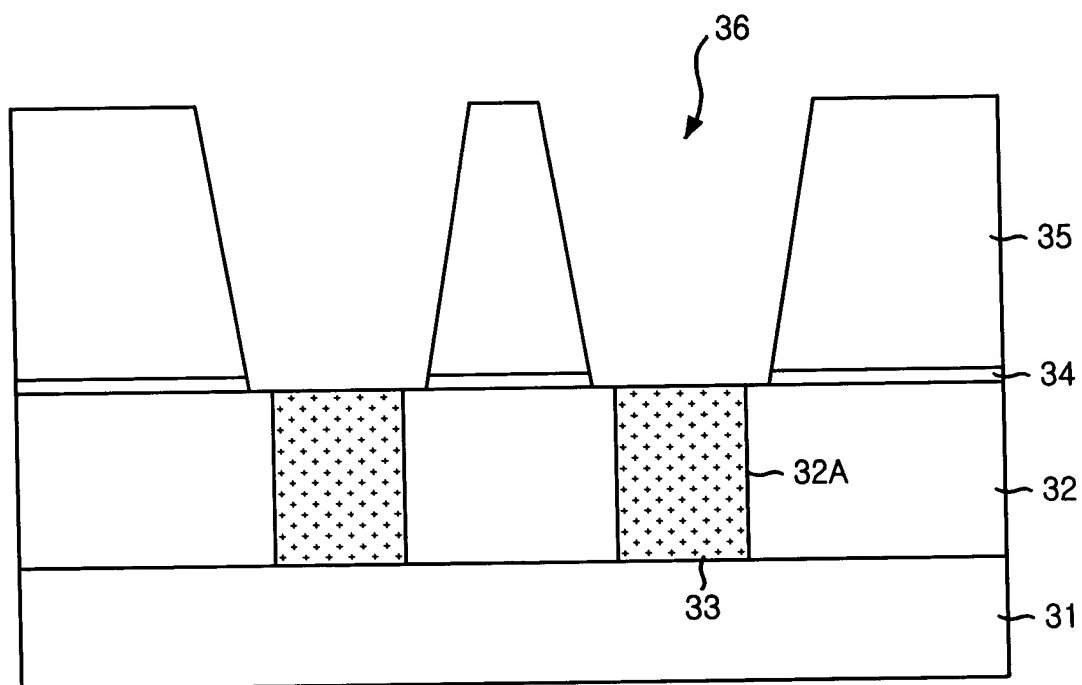


FIG. 4B

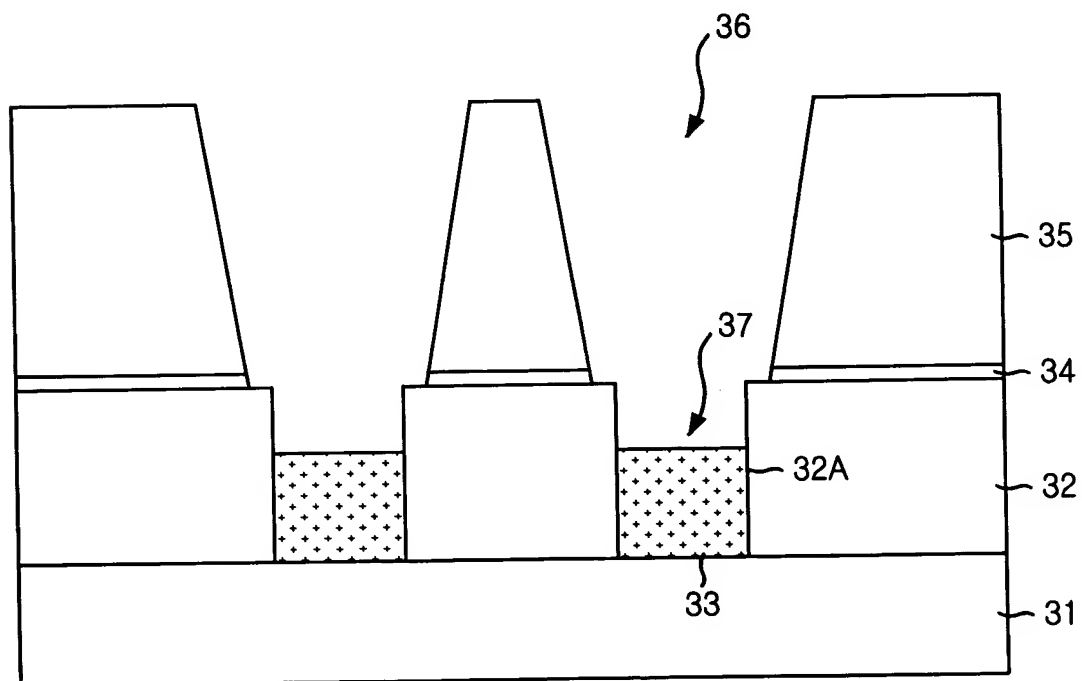


FIG. 4C

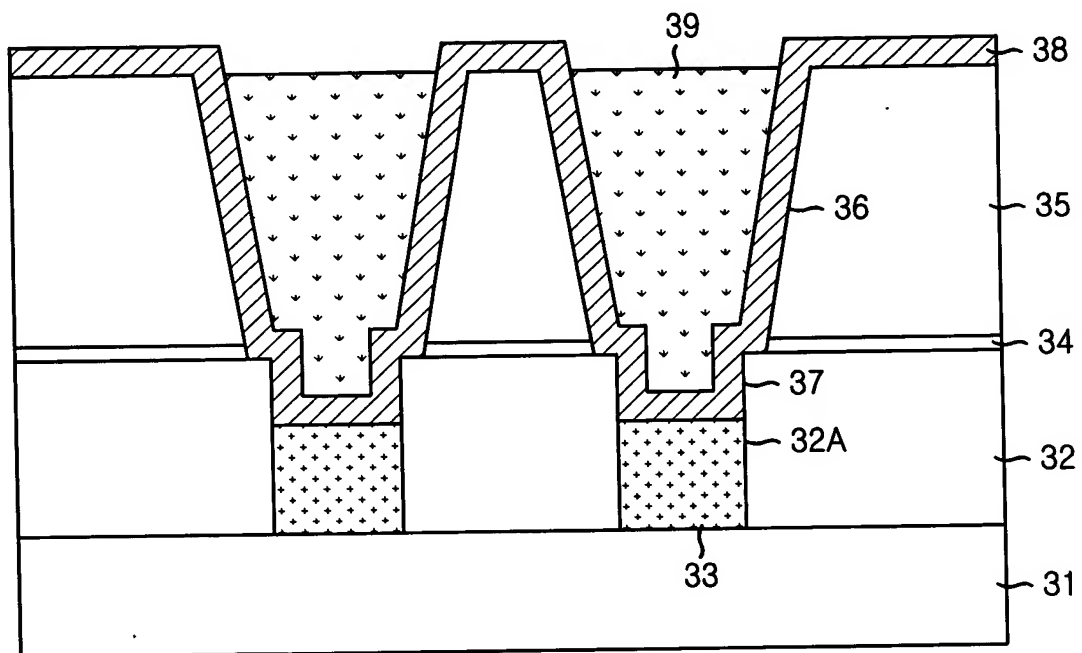


FIG. 4D

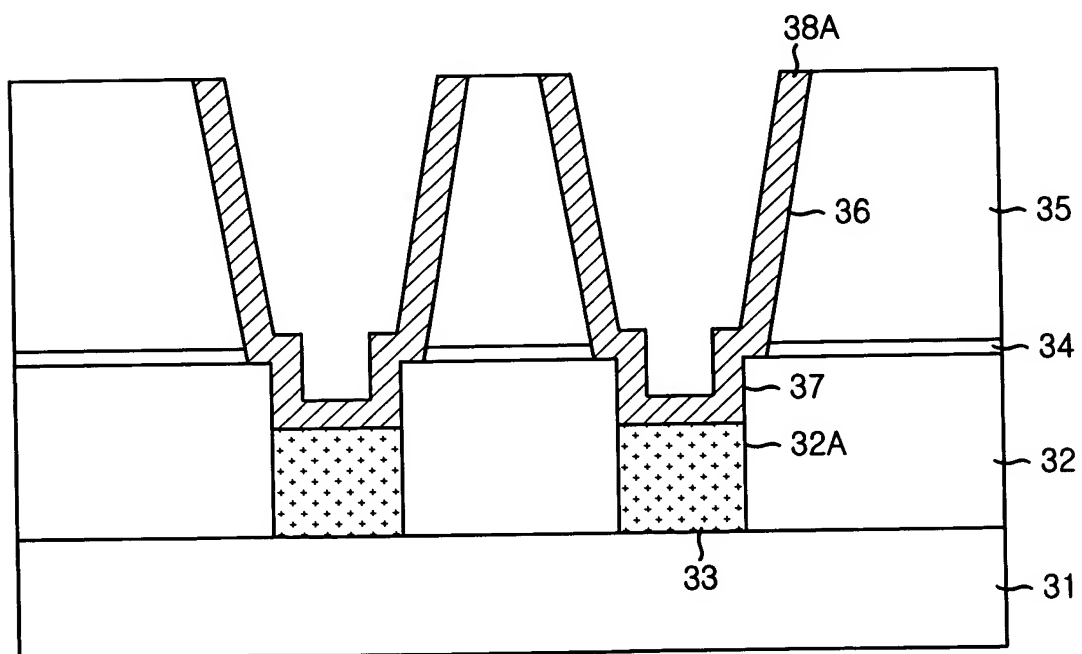


FIG. 4E

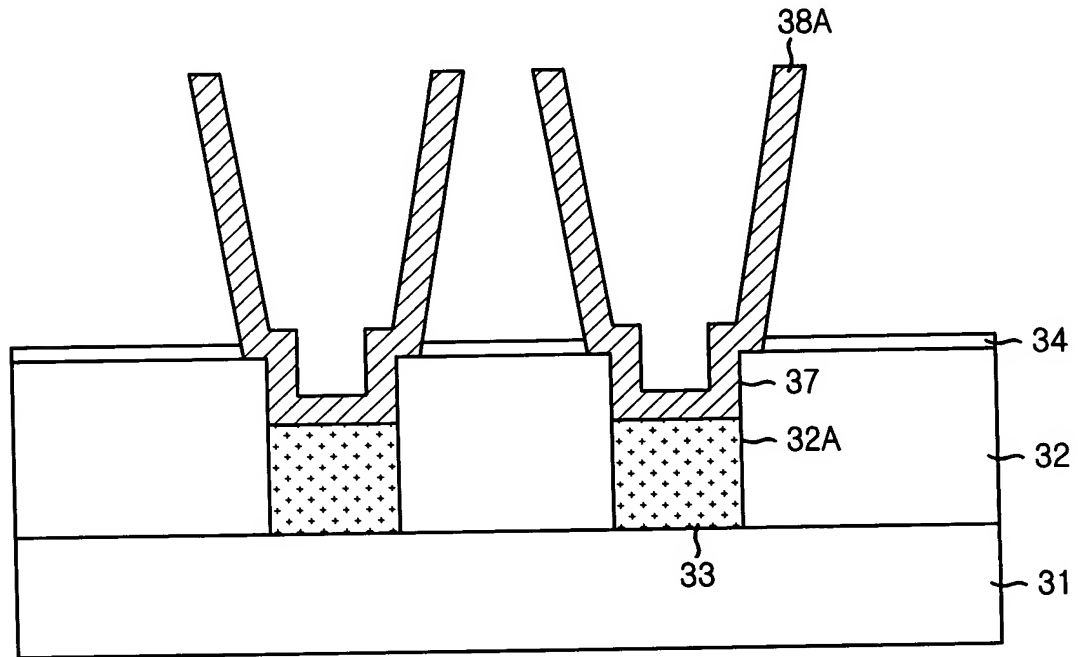


FIG. 4F

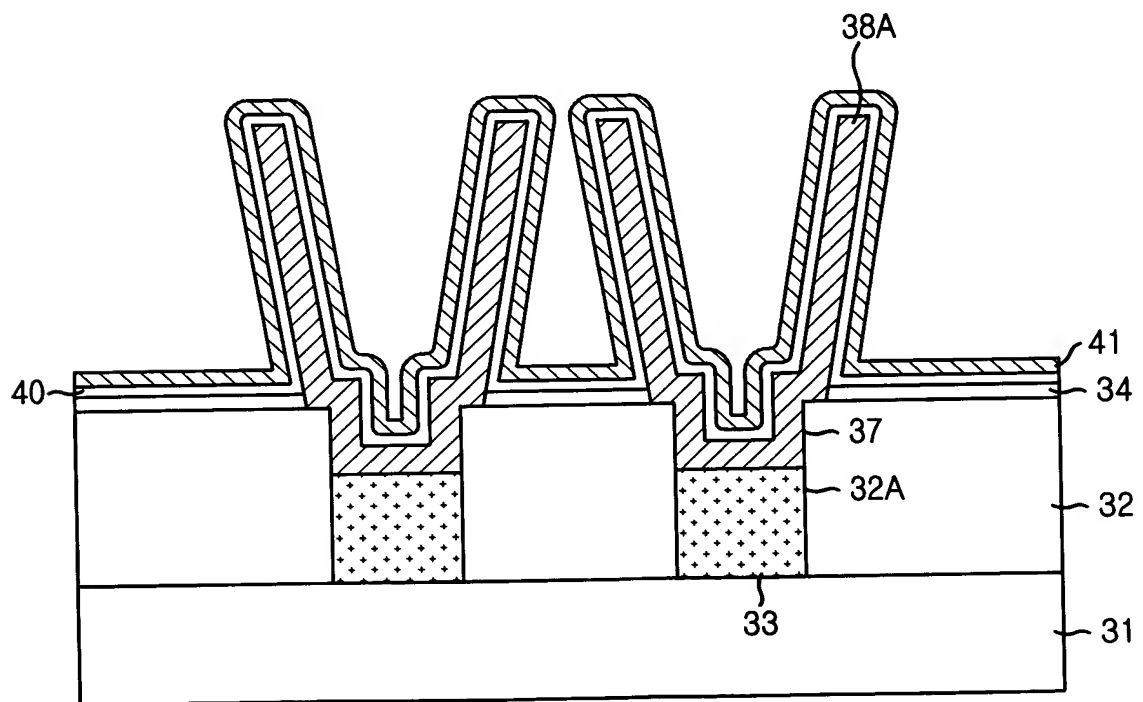


FIG. 5

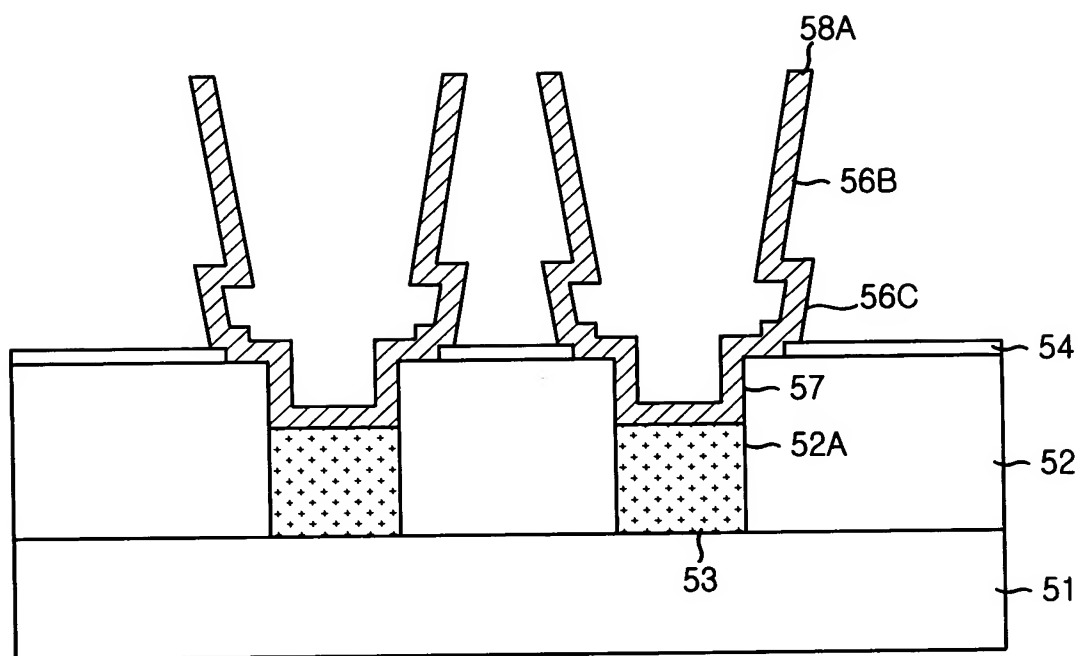


FIG. 6A

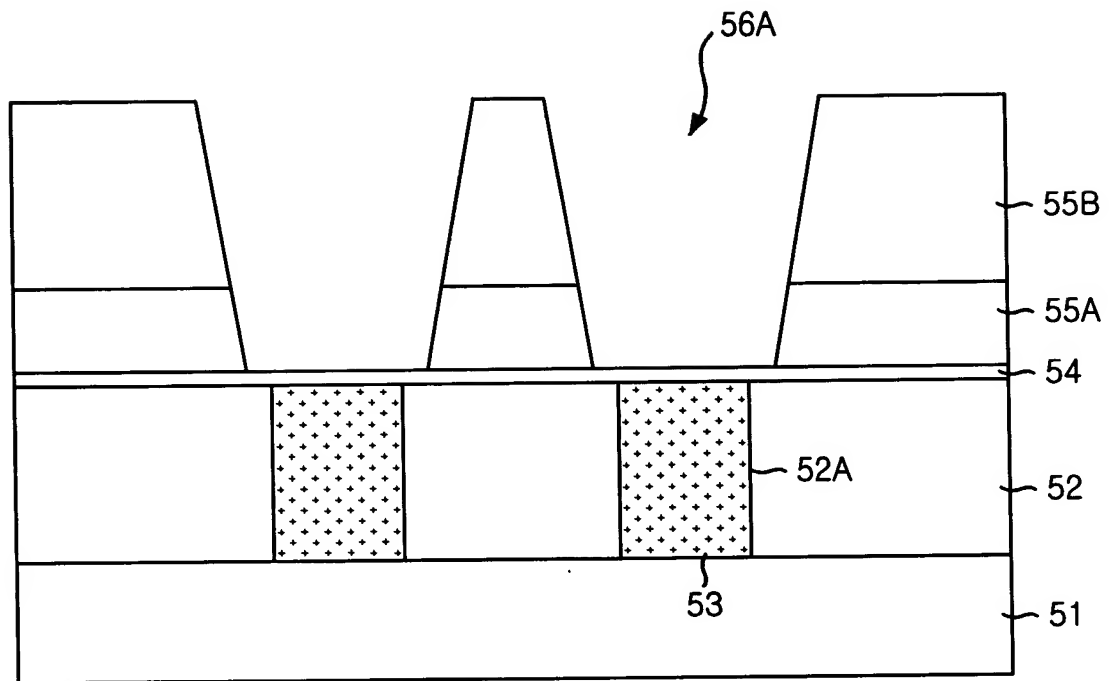


FIG. 6B

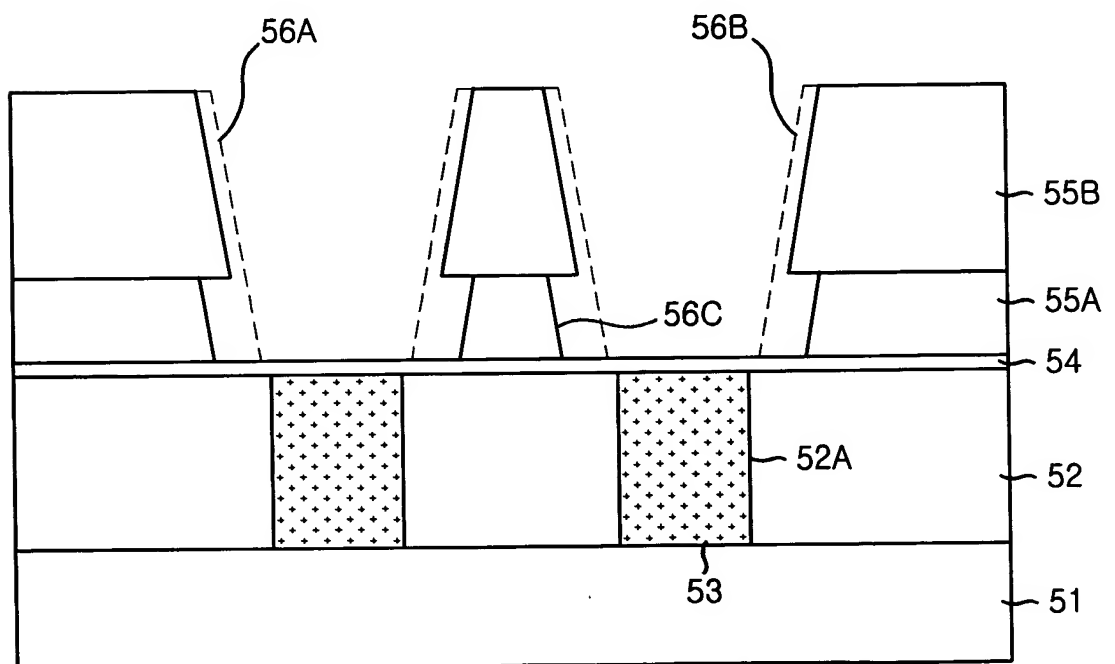


FIG. 6C

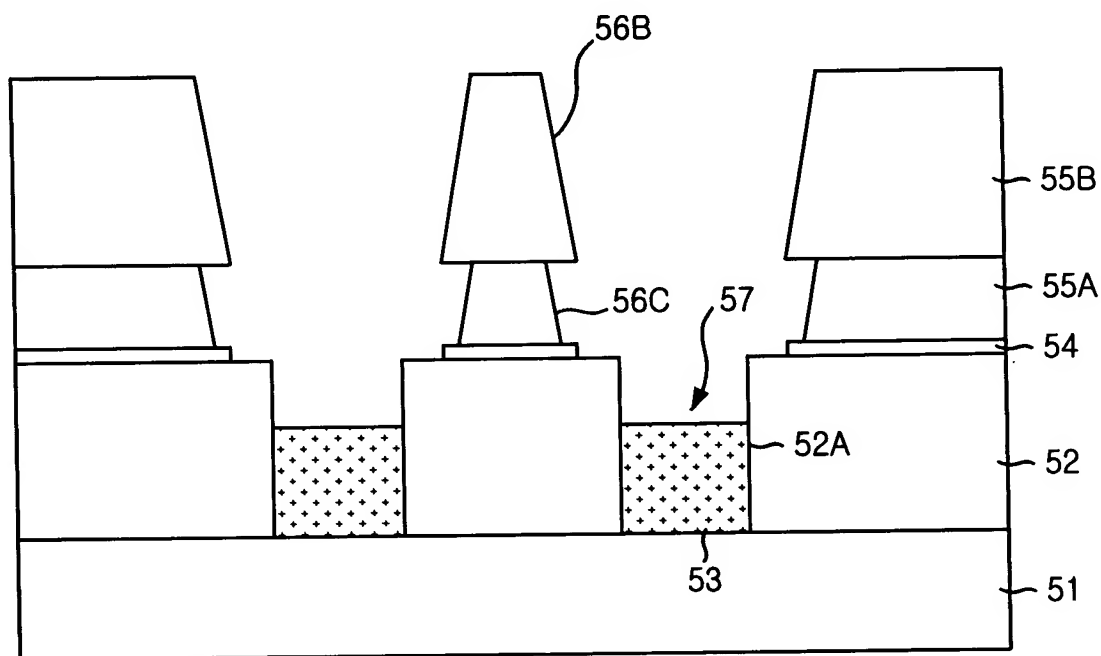


FIG. 6D

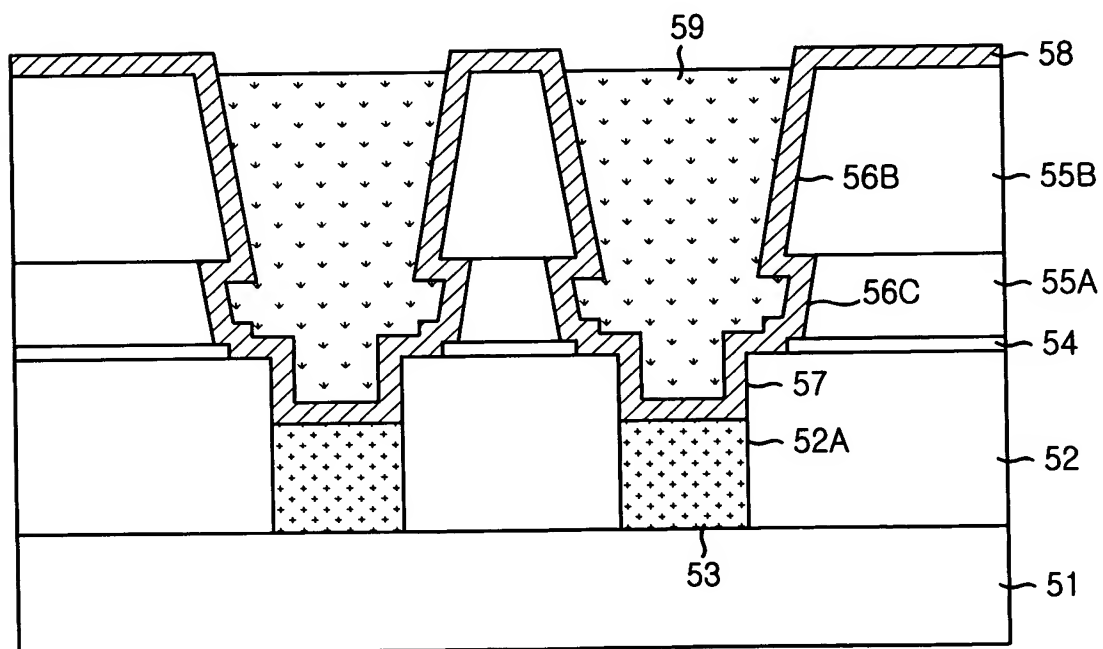


FIG. 6E

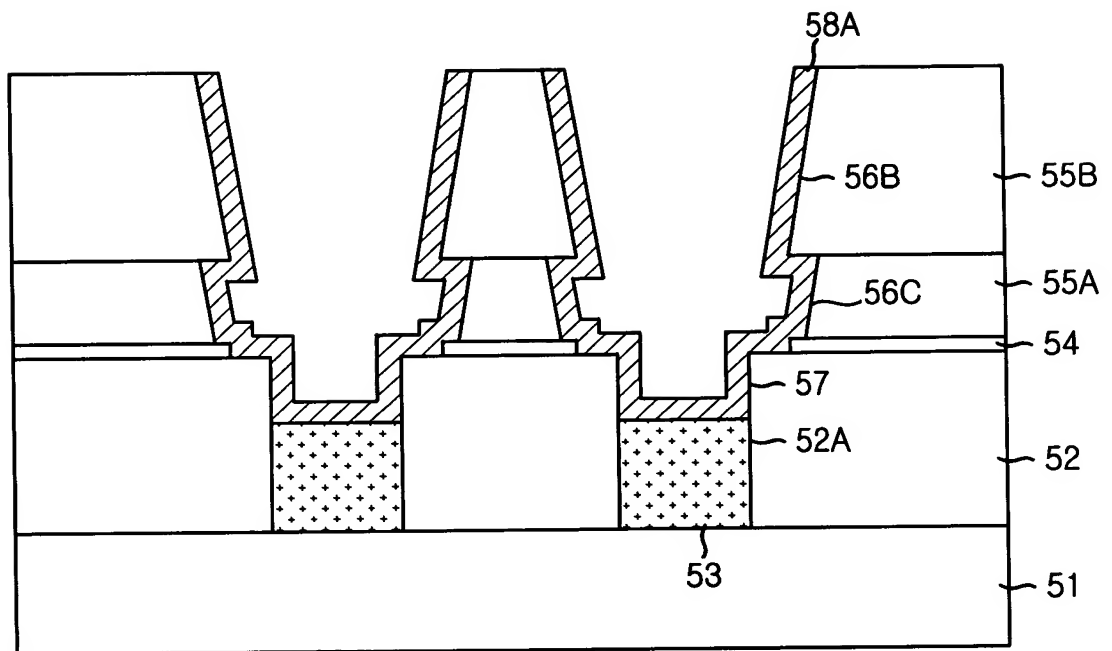
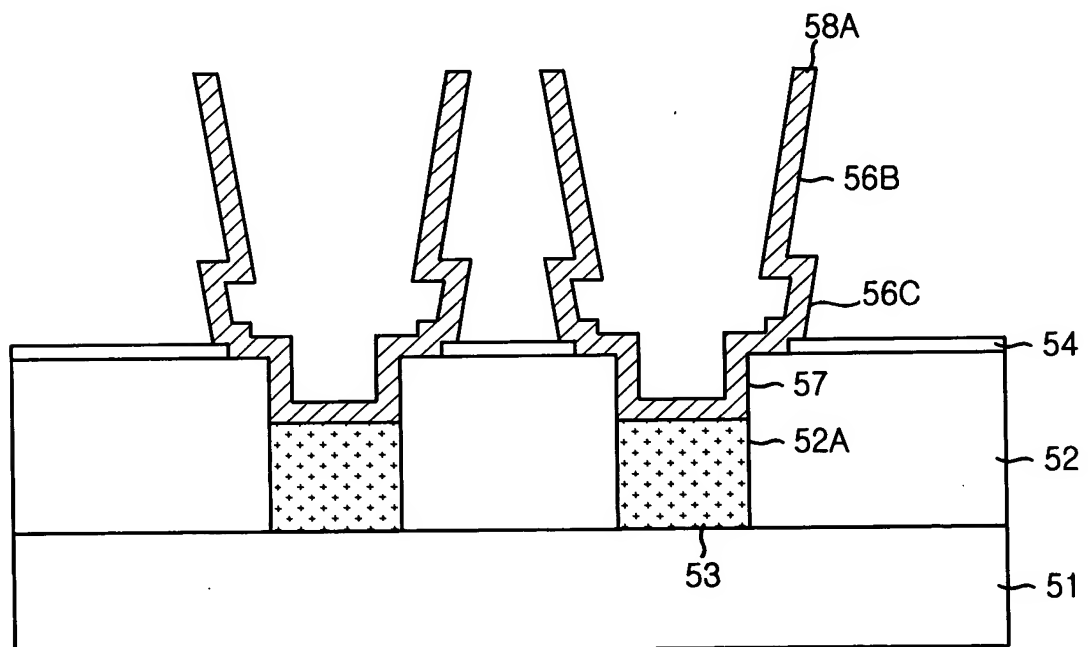


FIG. 6F



This cross-sectional view shows a semiconductor device with a multi-layered substrate. The substrate consists of a bottom layer 51, a middle layer 52, and a top layer 54. A patterned layer 53 is located within the middle layer 52, with a specific region labeled 52A. Conductive structures 57 are formed on the top layer 54, featuring a complex, stepped profile. A conductive layer 60 is positioned on the left side of the device. A conductive structure 58A is shown on the right side, extending upwards from the top layer 54. The device is shown in a cross-sectional view, with various layers and structures labeled with reference numerals.

FIG. 7

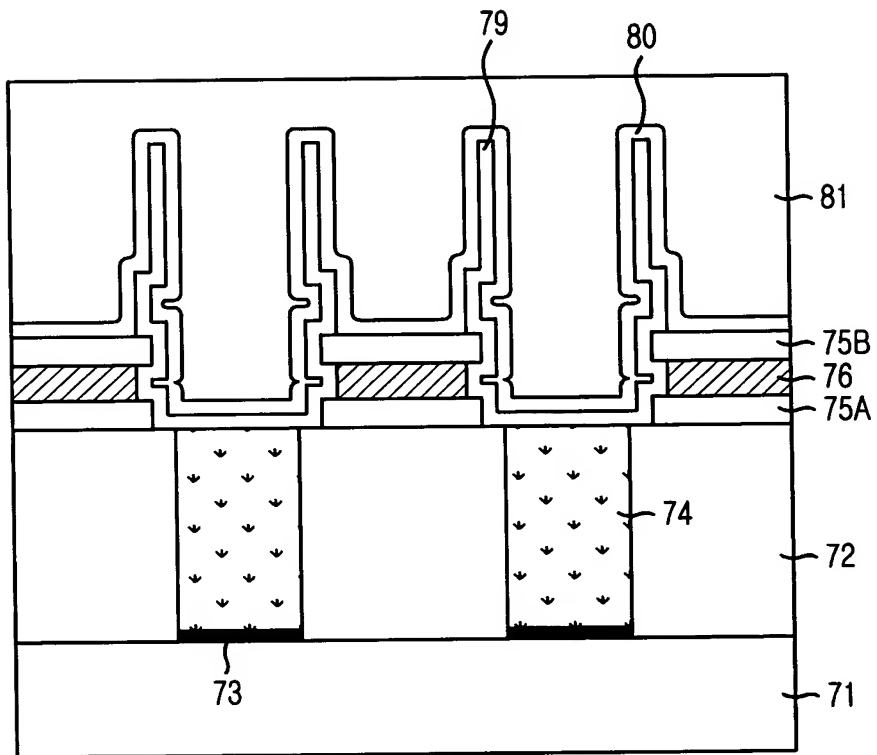


FIG. 8A

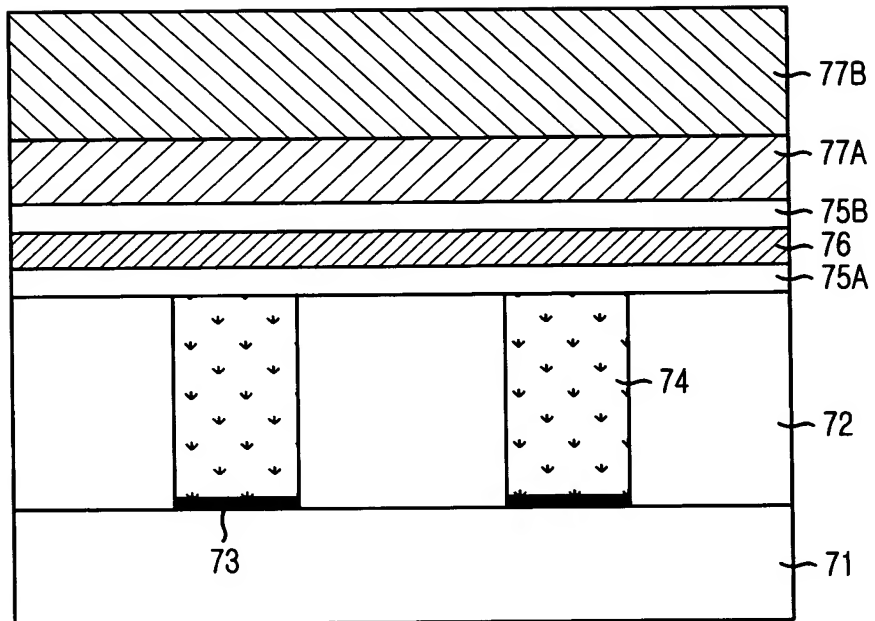


FIG. 8B

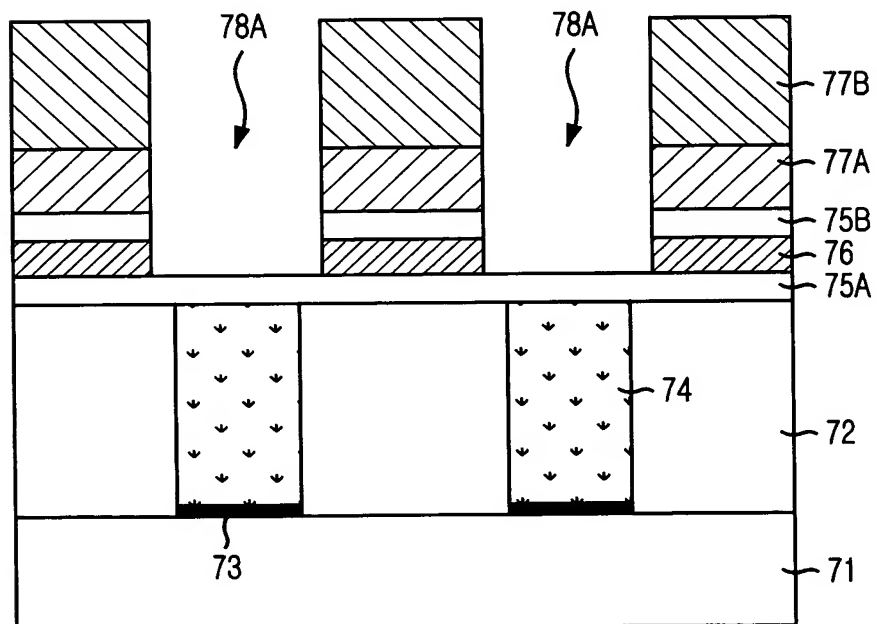


FIG. 8C

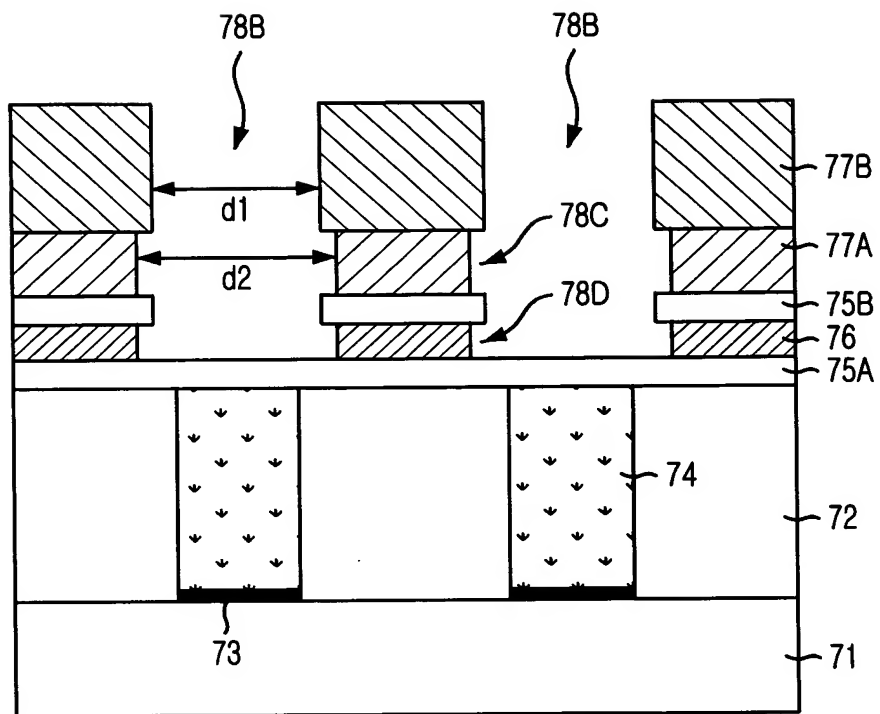


FIG. 8D

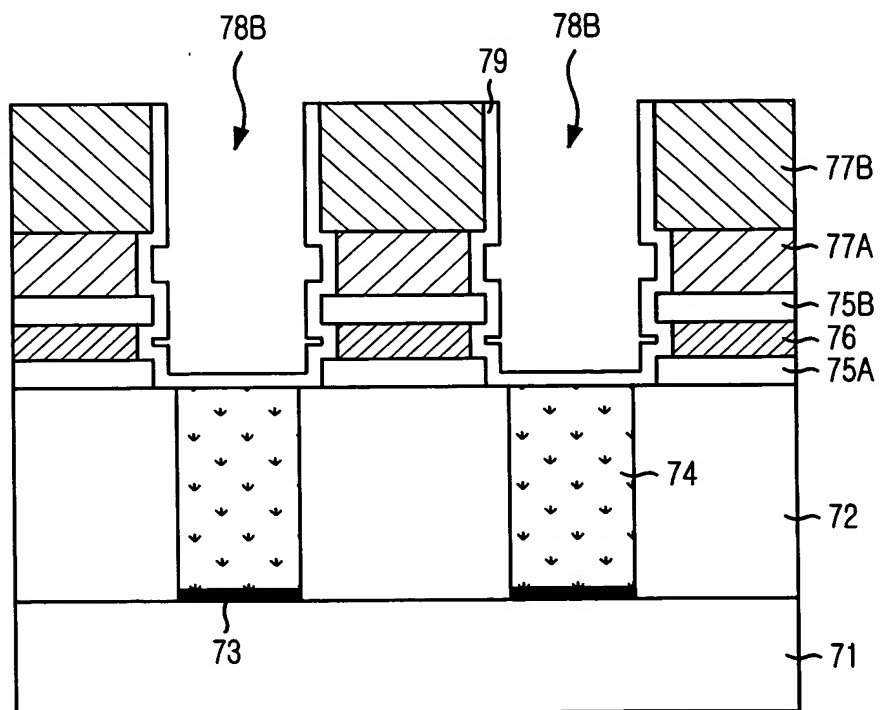


FIG. 8E

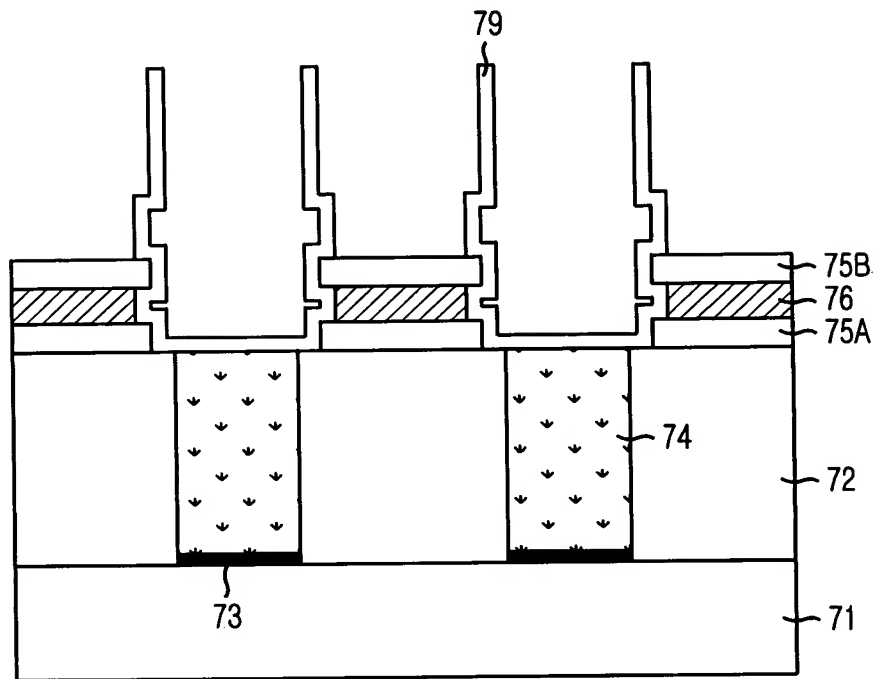


FIG. 8F

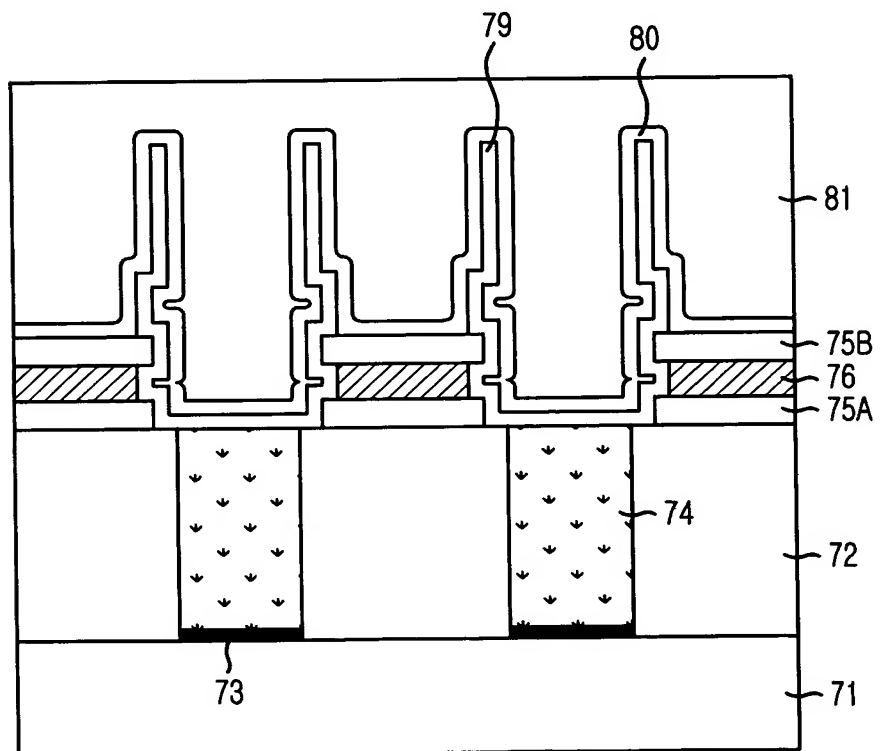


FIG. 9

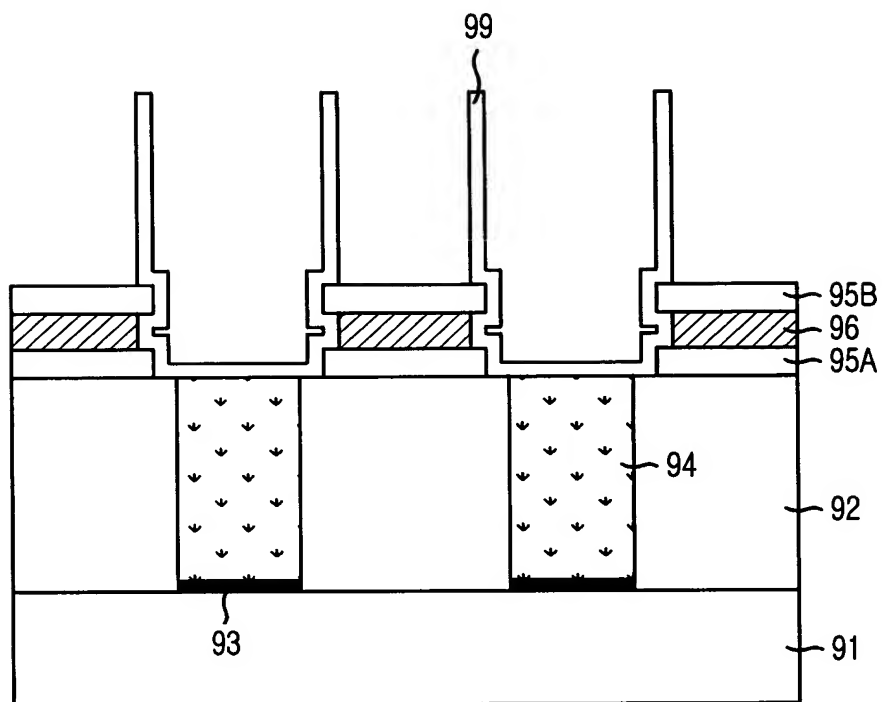


FIG. 10A

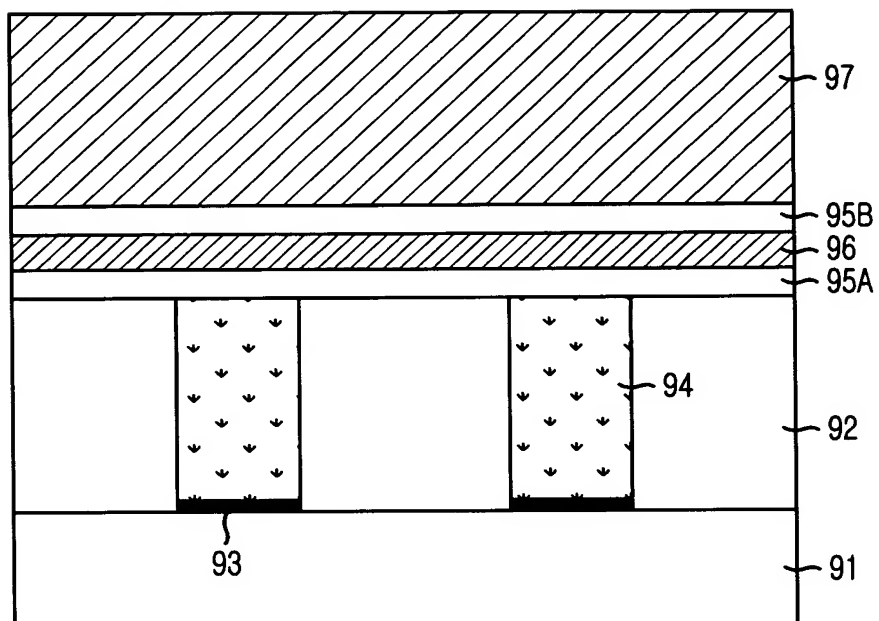


FIG. 10B

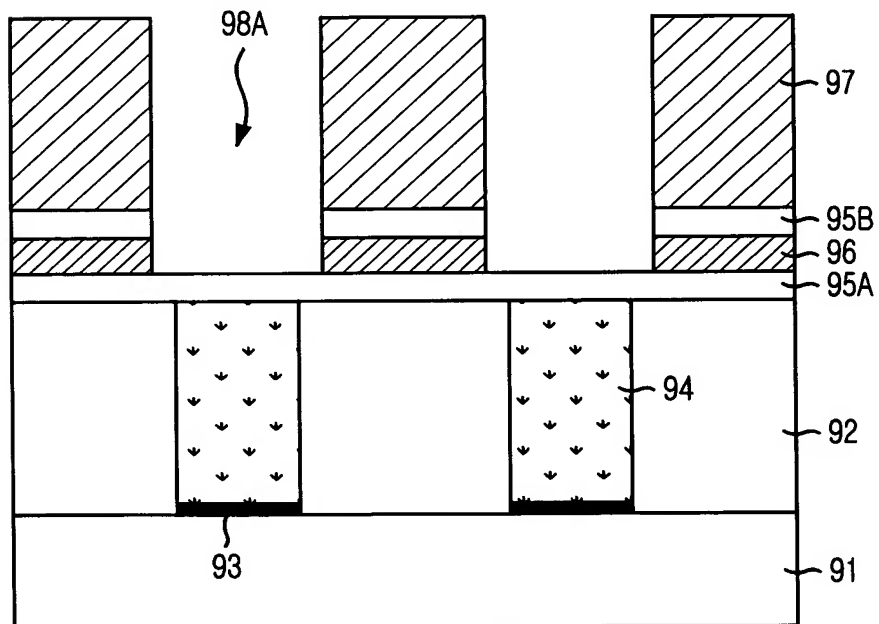


FIG. 10C

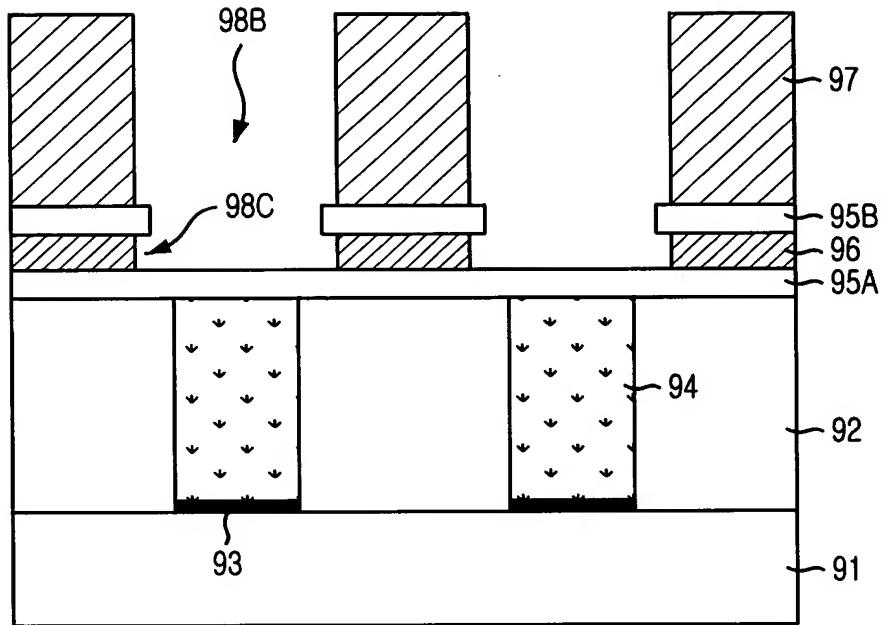


FIG. 10D

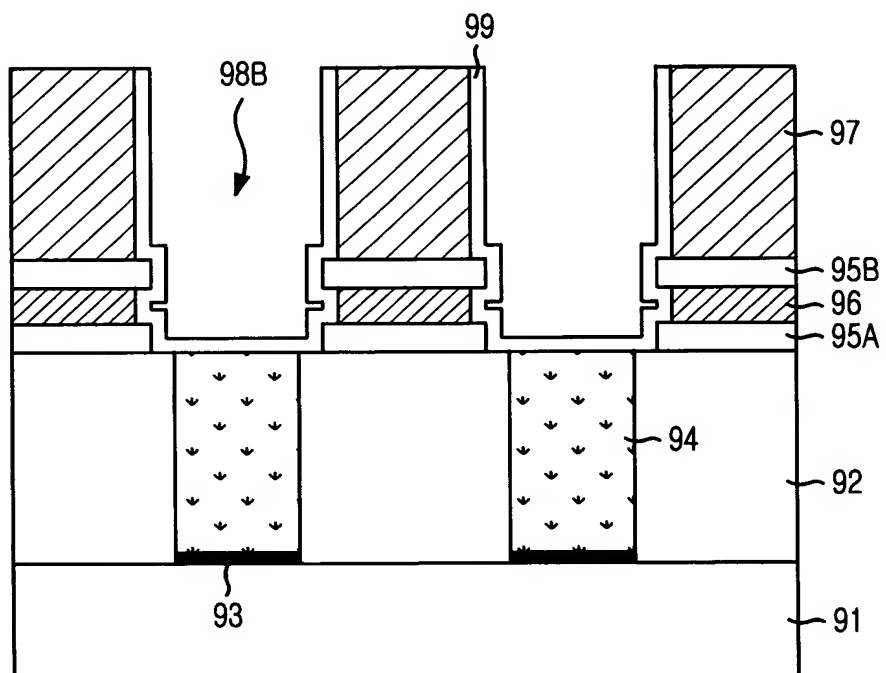


FIG. 10E

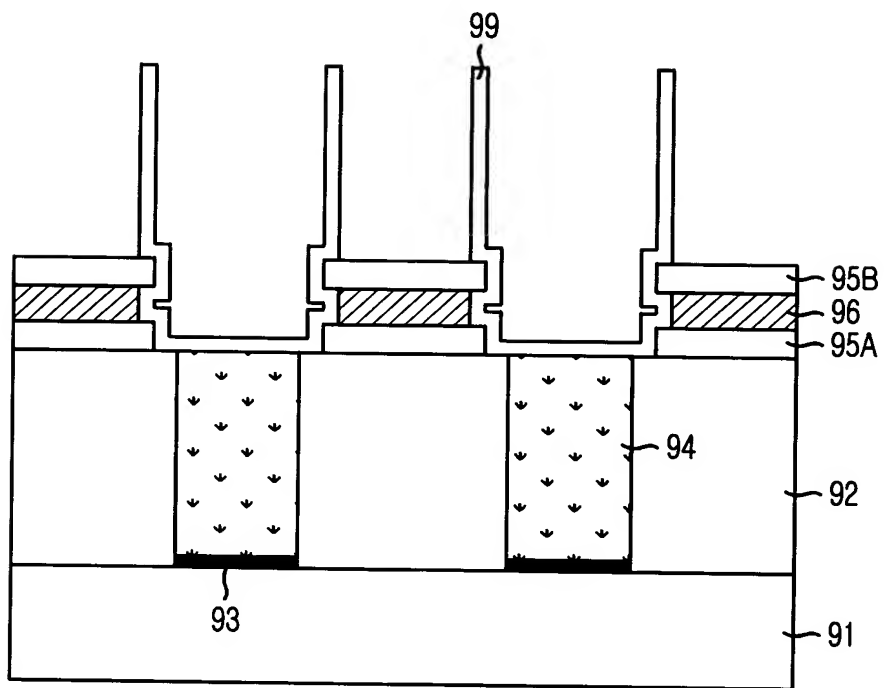


FIG. 10F

